Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-56 (canceled)

Claim 57 (new): A closed circuit video system that utilizes shared video memory, said system having:

a plurality, N, of image capture devices each producing a corresponding video signal so as to define a plurality of N video signals;

a circuit, responsive to said plurality of video signals, which in response to a selection control signal, routes a specific group, M, of selected ones of said video signals produced by M respective ones of the N image capture devices to associated output devices, where M and N are positive integers; and

wherein said circuit comprises:

a separate memory for each one of said M video signals, said separate memory implements a multi-functional shared store for its associated one of the M image capture devices, through which said separate memory supports video processing functionality associated with standard shutter imaging and slow shutter imaging as well as video processing functionality for other operations provided through said circuit such that said separate memory eliminates a need to have a separate frame store situated within or proximate to said associated one image capture device to implement slow shutter imaging, wherein, during standard shutter imaging

and slow shutter imaging, the separate memory is updated at a field rate appropriate to said associated one image capture device and read out at a rate appropriate to an image store function; and

said separate memory communicatively interacts with said associated one image capture device through which said associated one image capture device specifies, in response to whether said associated one image capture device is functioning in said standard or slow shutter imaging, if the separate memory should then update its video contents or not in response to a corresponding one of the video signals then being produced by said associated one image capture device.

Claim 58 (new): The system recited in claim 57 wherein the circuit comprises a frame grabber, an N x M video recording multiplexer, an N x M video matrix switch or an N x M video selector.

Claim 59 (new): The system recited in claim 58 wherein said associated one image capture device comprises a video camera or any other device that produces a video source signal.

Claim 60 (new): The system recited in claim 58 wherein said communicative interaction between said associated one image capture device and said separate memory occurs through bi-directional signaling there between.

Claim 61 (new): The system recited in claim 60 wherein said separate memory comprises a dual-ported memory.

Claim 62 (new): The system recited in claim 60 wherein said output devices comprise a plurality of video monitors.

Claim 63 (new): The system recited in claim 62 wherein said output devices include at least one video recorder.

Claim 64 (new): The system recited in claim 60 wherein the circuit synchronizes capture and refresh display of images from said one video signal produced by said associated one of the image capture devices when said associated one image capture device is operating in a slow shutter image processing mode.

Claim 65 (new): The system recited in claim 60 wherein the bidirectional signaling comprises a write control signal produced by said associated one image capture device, wherein the write control signal is a don't write signal.

Claim 66 (new): The system recited in claim 65 wherein said associated one image capture device comprises a video camera or any other device that produces a video source signal.

Claim 67 (new): The system recited in claim 65 wherein said separate memory comprises a dual-ported memory.

Claim 68 (new): The system recited in claim 65 wherein said output devices comprise a plurality of video monitors.

Claim 69 (new): The system recited in claim 68 wherein said output devices further comprise at least one video recorder.

Claim 70 (new): The system recited in claim 65 wherein the bidirectional signaling further comprises an enable-slow-shutter signal to enable operation of a slow-shutter mode of an image sensor associated with said associated one image capture device, and the write control signal is a don't-write signal when slow-shutter imaging is enabled in said associated one image capture device and the image sensor has not accumulated an image for a predefined slow-shutter speed.

Claim 71 (new): The system recited in claim 65 wherein the write control signal is separate from said one video signal.

Claim 72 (new): The system recited in claim 65 wherein the write control signal is superimposed on said one video signal.

Claim 73 (new): The system recited in claim 65 wherein a control signal within said bidirectional signaling is implemented through a unique voltage level superimposed on said one video signal.

Claim 74 (new): The system recited in claim 65 wherein a control signal within said bidirectional signaling is a pulse occurring during a vertical blanking interval of said one video signal.

Claim 75 (new): The system recited in claim 74 wherein said pulse has one or more predefined pulse widths that specify respective operating modes of said one image capture device.

Claim 76 (new): The system recited in claim 70 wherein the circuit further comprises:

an enable-detector circuit to detect the enable-slow-shutter signal; and

a generate-don't-write-signal circuit to generate the don't-write signal.

Claim 77 (new): The system recited in claim 76 wherein the circuit further comprises:

a generate-enable signal circuit to generate the enable-slow-shutter signal; and

a detect-don't-write-signal circuit to detect the don't-write signal, wherein the separate memory maintains a stored image frame in the separate memory when the detect-don't-write-signal circuit detects the don't-write signal.

Claim 78 (new): A closed circuit video system that utilizes a shared image store, said system having:

a plurality, N, of image capture devices, each producing a corresponding video signal so as to define a plurality of N video signals;

a circuit, responsive to said plurality of video signals, which in response to a selection control signal, routes a specific group, M, of selected ones of said video signals produced by M respective ones of the N image capture devices to associated output devices, where M and N are positive integers; and

wherein said circuit comprises:

a shared image store operative in conjunction with an associated one of said M video signals produced by a corresponding one of the N image capture devices, said image

store implementing a multi-functional shared store for said associated one video signal, through which said image store provides video storage functionality to support both a predefined image store operation and a predefined image processing operation by selectively operating in a first or second mode, respectively, such that said shared image store eliminates a need to have a separate frame store memory situated within or proximate to said corresponding one image capture device, said image store operation being different from said image processing operation; and

said image store communicatively interacts with said corresponding one image capture device through which said corresponding one image capture device instructs said shared image store to operate in said first or second mode so as to provide video storage functionality appropriate to either said image storage operation or said image processing operation as then required by current operation of said corresponding one image capture device.

Claim 79 (new): The system recited in claim 78 wherein the circuit comprises a frame grabber, an N x M video recording multiplexer, an N x M video matrix switch or an N x M video selector.

Claim 80 (new): The system recited in claim 79 wherein said associated one image capture device comprises a video camera or any other device that produces a video source signal.

Claim 81 (new): The system recited in claim 79 wherein said communicative interaction between said associated one image capture device and said separate memory occurs through

bi-directional signaling there between, and said first and second modes being write and don't write, respectively.

Claim 82 (new): The system recited in claim 81 wherein said output devices comprise a plurality of video monitors.

Claim 83 (new): The system recited in claim 82 wherein said output devices further comprise at least one video recorder.

Claim 84 (new): The system recited in claim 81 wherein the circuit synchronizes capture and refresh display of images from said one video signal produced by said associated one of the image capture devices when said associated one image capture device is operating in a slow shutter image processing mode.

Claim 85 (new): The system recited in claim 81 wherein the bidirectional signaling comprises a write control signal produced by said associated one image capture device, wherein the write control signal is a don't write signal.

Claim 86 (new): The system recited in claim 85 wherein the bidirectional signaling further comprises an enable-slow-shutter signal to enable operation of a slow-shutter mode of an image sensor associated with said associated one image capture device, and the write control signal is a don't-write signal when slow-shutter imaging is enabled in said associated one image capture device and the image sensor has not accumulated an image for a predefined slow-shutter speed.

Claim 87 (new): The system recited in claim 85 wherein the write control signal is separate from said one video signal.

Claim 88 (new): The system recited in claim 85 wherein the write control signal is superimposed on said one video signal.

Claim 89 (new): The system recited in claim 85 wherein a control signal within said bidirectional signaling is implemented through a unique voltage level superimposed on said one video signal.

Claim 90 (new): The system recited in claim 85 wherein a control signal within said bidirectional signaling is a pulse occurring during a vertical blanking interval of said one video signal.

Claim 91 (new): The system recited in claim 90 wherein said pulse has one or more predefined pulse widths that specify respective operating modes of said one image capture device.

Claim 92 (new): The system recited in claim 86 wherein the circuit further comprises:

an enable-detector circuit to detect the enable-slow-shutter signal; and

a generate-don't-write-signal circuit to generate the don't-write signal.

Claim 93 (new): The system recited in claim 92 wherein the circuit further comprises:

a generate-enable signal circuit to generate the enable-slow-shutter signal; and

a detect-don't-write-signal circuit to detect the don't-write signal, wherein the separate memory maintains a stored image frame in the separate memory when the detect-don't-write-signal circuit detects the don't-write signal.